



USB 2.0 Device Controller

PRODUCT BRIEF

Overview Features

Highly Configurable Technology Independent System Validated

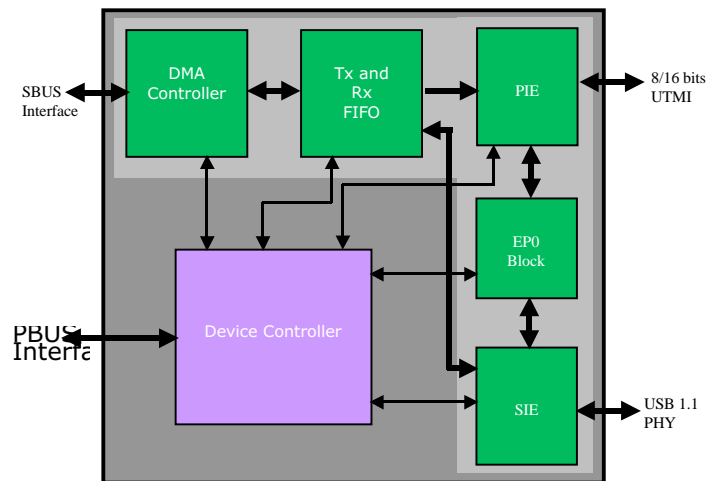
CUSB2DEV is a highly configurable USB 2.0 device Controller core. It can be easily integrated into ASIC as well as FPGA. The PBUS & SBUS interface allows the core to be integrated with any other applications, which requires USB 2.0 interface. The controller architecture is carefully tailored for high throughput, low latency, better reliability, and low power consumption.

The controller's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. The hardware configurable feature such as number of endpoints allow the core to be used by multiple applications which can share the USB bus bandwidth among them through SBUS interface.

GDA solution allows the licensees to easily migrate to FPGA, Gate array and Standard cell technologies optimally. Its backend interface makes it easy to be integrated into wide range of applications. The CUSB2DEV core is highly configurable, fully synchronous, and highly modular design to meet the requirement of a reusable IP in SoC designs.

GDA's CUSB2DEV solution leverages years of experience in 10/100/1000 Mbps MAC, SPI-4, PCI-X, PCI Express and Hyper Transport technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and inter operability.

- USB 2.0 compliant
- Supports High/Full/Low speed devices
- UTMI 8-bit Unidirectional compliant
- Optional UTMI 16-bit bi-directional support
- Optional USB 1.1 PHY support
- Optional DMA controller, configurable build-in FIFO for each endpoint.
- Direct FIFO interface in absence of DMA
- Hardware configurable number of endpoints
- Software configurable endpoint number, type and packet size
- Supports 4 configurations, 4 interfaces, 4 alternative Interfaces and 16 endpoints
- Suspend, Resume and Wakeup logic is provided
- Optional Endpoint Zero block: supports all standard requests except set Descriptor command, and sync frame command.





USB 2.0 Device Controller

Visit: www.gdatech.com

Call: 408.432.3090

Fax: 408.432.3091

Email: ip@gdatech.com

Write: GDA Technologies
1010 Rincon Cir
San Jose, CA 95131

Specifications

Configurable Options

- Optional DMA controller
- Optional Endpoint Zero support
- Optional 16-bit bi-directional UTMI interface
- Optional USB 1.1 Legacy PHY Support
- Optional number of endpoints

Design Attributes

- Fully synchronous design
- Highly modular design
- Separate hierarchy for optional logic
- 30/60MHz clock on UTMI interface and up to 100MHz on system interface
- 32-bit SBUS, PBUS and 36-bit FIFO interface

Product Package

- RTL view in Verilog HDL
- Comprehensive functional test bench
- Synthesis scripts
- USB 2.0 test suite
- Training and support programs

Documentation

- User manual
- Synthesis Guide
- Design document
- Verification Guide

Status : Silver
Availability : Now
Language : Verilog HDL
Synthesis : Ambit/Synopsys/Synplify
Simulation : Cadence's Verilog-XL/NC Verilog
Technology : 0.18u or better

GDA Technologies reserves the right to change this document without prior notice and disclaim all warranties. It is the recipient's duty to confirm with GDA Technologies' Engineering Department specifications before proceeding with a product design.

GDA Technologies, CUSBDEV2 Core and the GDA Technologies logo are trademarks of GDA Technologies, Inc.
Patents and Patents pending.

©2003 GDA Technologies, Inc. San Jose, CA. All rights reserved.

August 2003 Version 1.0

