



# Configurable PCI-X Core

## PRODUCT BRIEF

Overview

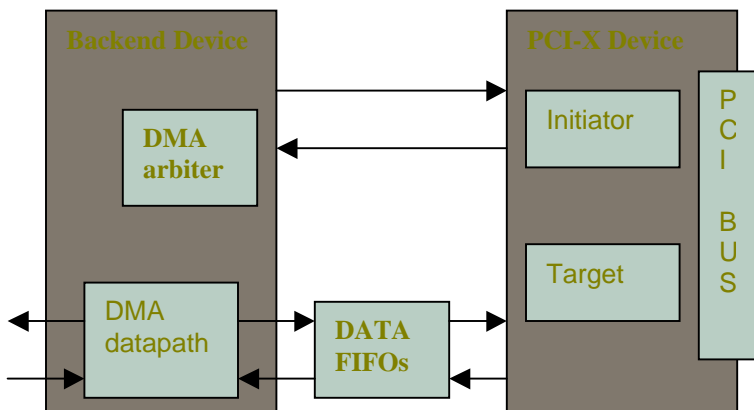
Features

Highly Configurable  
High-Speed  
Low-Area

CPCI-X is a PCI-X compliant design scoped to provide a system interface to any networking application involving streaming data transfers. It basically focuses on the transfer of large chunks of data between the DMA unit of backend and the host memory adhering to PCI-X protocol (Rev 1.0) which is downward compatible with PCI protocol(Rev 2.2) and also on configuring the backend registers through memory accesses. The core provides a DMA arbitrator (optimized for two DMA controllers) and the initiator-target pair to handle these transactions as per the PCI-X(Rev 1.0) protocol.

- Fully compliant with PCI-X protocol (Rev 1.0)
- Posting for outbound memory writes
- Basic power management supported in PCI-X mode
- MSI capability
- 64/32 addressing capability
- 64/32 data transfer capability
- Medium decode time supported for target
- Flexible master-target interface that can be customized for varied data streaming applications
- Fully synchronous design
- PCI-X bus operation up to 133MHz
- Good debugging support for erroneous transactions.

### PCI-X Reference Model



Separable backend and pci-x devices.

### Configurable Features

#### Hardware configurable Features

- Separable backend and pci-x devices
- Separable initiator and target cores
- Configurable FIFO depth
- Subsystem ID and subsystem vendor ID can be either hardwired or entered through monitor interface.





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## Software configurable Features

- Choosing between interrupt pin and MSI
- Address space below or above 4 GB
- All others as specified in the protocol
- Soft reset

## Unique Features

- A transaction once taken in by the core will be finished taking care of any number of disconnects with or without data and retries in PCI mode.
- The possibility of data reordering in case of disconnects is taken care of and the user interface is assured of data integrity while placing data on the bus with respect to memory location addresses in PCI mode.
- All disconnects (ADB or otherwise) or retries in PCI-X mode will be dealt with properly so that the transaction that is taken in by the core is completed by all means.

## Unique Features contd.

- Any read transaction taken in PCI-X mode is initiated according to the size limitation imposed on the core by the host in the control register and the whole transaction is completed according to the dynamic size limitations imposed coordinating interm disconnects and splits.
- The possibility of data reordering because of part of the transaction completed by initiator and another part by the target as split completion, is taken care of and the user interface is assured of data integrity.
- All the above unique features result in a direct plug and play kind of user interface relieved of all the hassles happening on the PCI bus interface.





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**Visit:** [www.gdatech.com](http://www.gdatech.com)

**Call:** 408.432.3090

408.432.0660

**Fax:** [ip@gdatech.com](mailto:ip@gdatech.com)

**Email:** GDA Technologies

1010 Rincon Cir

**Write:** San Jose, CA 95131.

## Specifications

### Design Attributes

Highly modular design

Fully synchronous, technology-independent design

64-bit wide internal data path

Clearly demarked clock domains

### Product Package

RTL code

Detailed design document

Verification environment

Test cases

Synthesis environment guide

### Documentation

User Guide

Verification guide

Synthesis Guide

**Status :** RTL Completed

**Availability :** Apr,2003

**Language :** Verilog HDL

**Synthesis :** Ambit, Xilinx

**Simulation :** Verilog-XL

**Technology :** 0.18u ASIC / FPGA

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