



Configurable Viterbi Decoder (CVD)

PRODUCT BRIEF

Overview

Features

Highly-Configurable Low-Area Depuncturing Support

CVD is a highly configurable architecture for design reuse. Viterbi decoders are widely used in digital communication systems. Depending on the application, CVD can be configured for specific code parameter requirements.

The design employs Add-Compare-Select (ACS) parallelism and pipelining for performance scalability. The trellis and pathmetric memory addressing is configured accordingly.

The design provides a real-time or bus input/output interface and a Bit Error Rate (BER) monitor. It also supports punctured symbol data input and synchronization. The design is modular, fully synthesizable and can be configured for the speed and area

- ❑ Highly Parameterized Viterbi Decoder
- ❑ Configurable architecture for performance scaling
- ❑ Supports throughput upto 8.3125 Mbps on 0.18 μ
- ❑ External Trellis Memory
- ❑ External Path Metric Memory
- ❑ Software Configurable through PPCI
- ❑ Optional PPCI for Input / Output
- ❑ Optional BER Monitor
- ❑ Node Synchronization based on pathmetrics normalization and BER
- ❑ Interrupts on Data availability, Synchronization error, Normalization and BER





Configurable Viterbi Decoder (CVD)

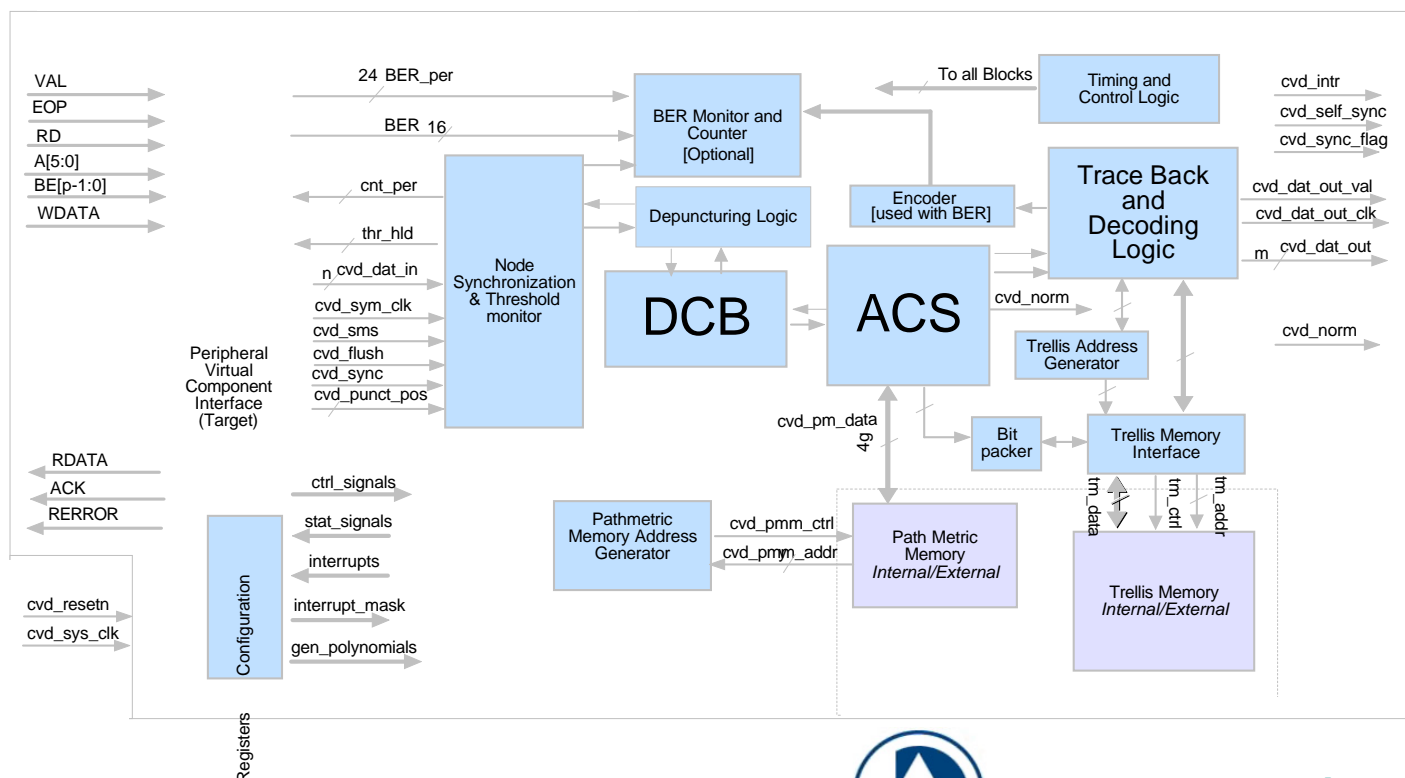
Specifications

Hardware Configurable Options

- ❑ Code rate [r] 1/2
- ❑ Punctured code rates 2/3 to 7/8
- ❑ Constraint Length K = 5 to 9
- ❑ Symbol data input in Serial or Parallel formats
- ❑ Puncturing format
- ❑ Hard decision decoding
- ❑ Configurable Precision of Path metrics
- ❑ Trace back depth
- ❑ External Depuncturing Support
- ❑ External memory support (for Path Metrics)
- ❑ Configurable sequential, hybrid or parallel ACS architecture
- ❑ Configurable Input-Output data interface supported (PVCi-PVCi, RT-PVCi, RT-RT)
- ❑ BER Monitor [Optional]

Software Configurable Options

- ❑ Programmable Generator Polynomial formats
- ❑ Internal or External synchronization option in RT-PVCi mode
- ❑ Software clear & flush
- ❑ Path metric / BER based synchronization option
- ❑ Programmable Interrupt mask
- ❑ Internal depuncturing bypass.
- ❑ Programmable BER window
- ❑ Programmable BER threshold





Configurable Viterbi Decoder

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Design Attributes

- Highly Modular and Parameterized Design
- Area-Efficient Reusable Soft Core
- Fully Synchronous to a Single Clock
- External Memory Support For Intermediate Metrics
- Active Low Asynchronous Reset
- Active High Synchronous Software Reset

Product Package

- RTL and Testbench Code
- Exhaustive Listing of Test cases
- Synthesis Scripts
- Code Coverage Scripts
- Parameter Generation Code and Run Scripts
- Detailed Documents

Documentation

- Design Documents
- Testbench Document
- Acceptance Test Guide
- User Guide (For Performing Simulation, Synthesis, Coverage)

Status : Design complete

Availability : June 2002

Language : Verilog

Synthesis : BuildGates

Simulation : Verilog-XL

Technology : 0.18u Standard

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