



Configurable UART

PRODUCT BRIEF

Overview Features

Highly Configurable Technology Independent System Validated

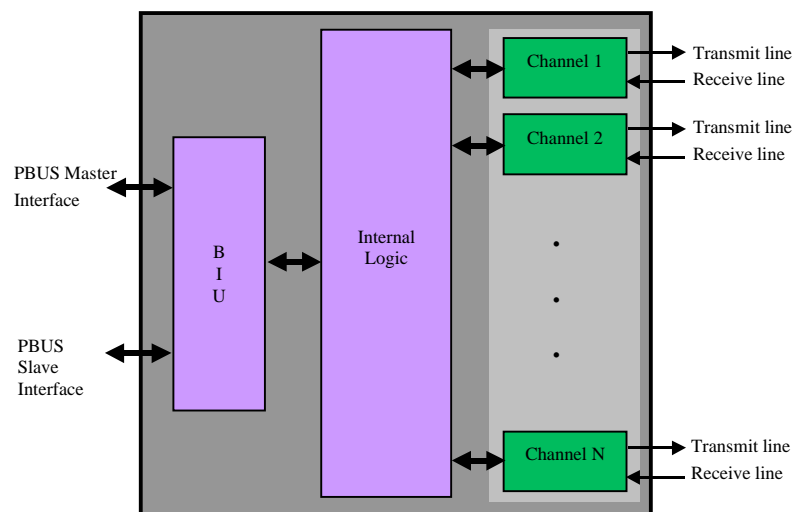
CUART is a configurable multi-channel Universal Asynchronous Receiver Transmitter Core, designed to be compatible with the Industry standard 16550 UART. CUART supports a maximum of 32 channels simultaneously and these channels can be individually configured and operated. The hardware configurable options allow core generation tailored to specific application needs. It can be readily integrated in many of the existing SOC environments.

In Master mode, CUART with out host CPU intervention can transfer data between the UART and Host memory. In Slave mode, data transfer can be either through polled or interrupt based. PBUS interface is used as the system interface. A separate PBUS interface is used for internal register access and for data transfers in slave mode.

The CUART provides modem control capability for each individual channel. In addition, two general-purpose output signals are provided for external device configuration. GDA's XMAC is a cost-effective, end-to-end system validated solution that allows the licensees to easily migrate to FPGA, Gate array and Standard cell technologies optimally.

GDA's CUART solution, leverages years of experience in creating reusable designs for Ethernet, PCI-Express, SPI-4, and Hyper Transport technologies and the expertise in creating system validated solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and interoperability.

- A full duplex independent multi-channel asynchronous receiver/transmitter
- Master/Slave modes for each receiver and transmitter
- Integrated DMA engine and arbitration logic in Master mode
- 16 character FIFOs for each receiver and transmitter
- Four different FIFO thresholds
- Programmable data formats - word length, stop bits and Parity
- Programmable baud rate for each receiver and transmitter
- Modem controls functions - CTS, RTS, DSR, DTR, RI and DCD
- PBUS bus compliant
- Power down mode
- Software compatible with 16550
- Parity, framing, and overrun error detection
- Internal diagnostic loop back mode
- Prioritized transmit, receive, line status and modem control interrupts.





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Specifications

Configurable Options

- No of Channels
- Master/Slave for Tx/Rx and for individual channel
- Optional FIFOs.
- Address and data bus widths.
- Software configurable data formats
- Baud rate selection

Design Attributes

- Fully synchronous design
- Technology independent design
- Highly modular design
- Highly configurable design

Product Package

- RTL code
- Automated and parameterized testbench
- Synthesis scripts

Documentation

- Design document
- Testbench Specification
- Synthesis guide
- User guide

Status : Gold [Silicon proven]

Availability : Now

Language : Verilog

Synthesis : Ambit/Synopsys DC

Simulation : Verilog XL

Technology : 0.18micron

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