



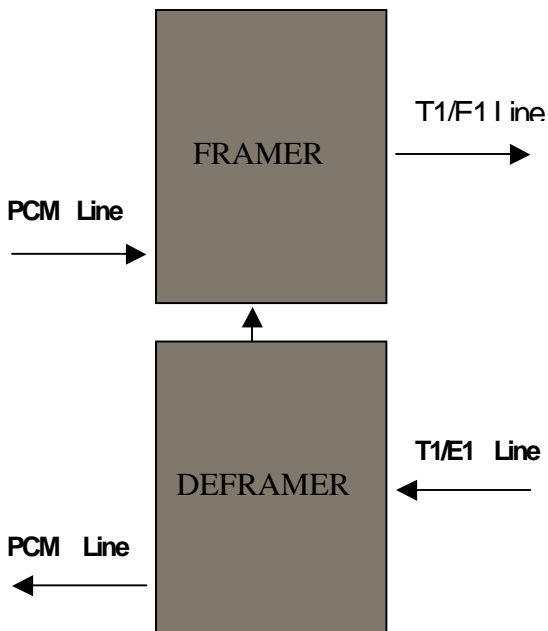
# Configurable T1/E1 Framer/Deframer

## PRODUCT BRIEF

### Overview Features

The T1/E1 framer multiplexes the PCM data, signaling data and data link data onto the T1/E1 line. The deframer de-assembles the PCM data, signaling data and data link data from the serial data received on the T1/E1 line. Alarms are generated at the de-assembler in accordance with the ITU-T

### T1/E1 Reference model



- ❑ Conforms to ITU-T recommendations, G.704, G.706 and G.775
- ❑ Fully independent framer and de-framer with feedback to framer from de-framer.
- ❑ T1 framer supports SF and ESF framing formats.
- ❑ Supports ABCD signaling in T1-ESF mode, AB signaling in T1-SF mode and channel associated signaling in E1 mode.
- ❑ Provides two frame/four frame controlled slip buffers with parameterized threshold for repeating and deleting frames.
- ❑ Fully synchronous design using multiple clocks, with asynchronous reset synchronized for different clocks.
- ❑ Supports CRC in T1-ESF and E1 framer/de-framer.
- ❑ Provides detection of Blue Alarm (AIS) and Red Alarm (Loss of synchronization by de-framer)
- ❑ Indicates occurrence of CRC errors, framing bit errors and controlled slips.
- ❑ Automatic internetworking between CRC-4 and non CRC-4 interfaces for E1 framer and de-framer as specified in ITU-T G.706





# Configurable T1/E1 Framer/Deframer

## Configurable features

### Hardware configurable features

- The core can be configured as either T1 or E1
- Slip buffer can be configured as two frame slip buffer or four frame slip b

### Software configurable features

- Robbed bit signaling (can be enabled or disabled).
- SF and ESF modes in T1

## Specifications

### Design Attributes

- Modular and Parameterized Design
- Fully synchronous, technology independent design

### Product Package

- RTL code
- Detailed design document
- Verification environment
- Test cases
- Synthesis environment guide

### Documentation

- User Guide
- Verification guide
- Synthesis Guide

**Status:** Complete

**Availability:** Now

**Language:** Verilog HDL

**Synthesis:** Ambit

**Simulation:** Verilog-XL

**Technology:** 0.18u Standard cell

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