



Smart Card Controller

PRODUCT BRIEF

Overview

Features

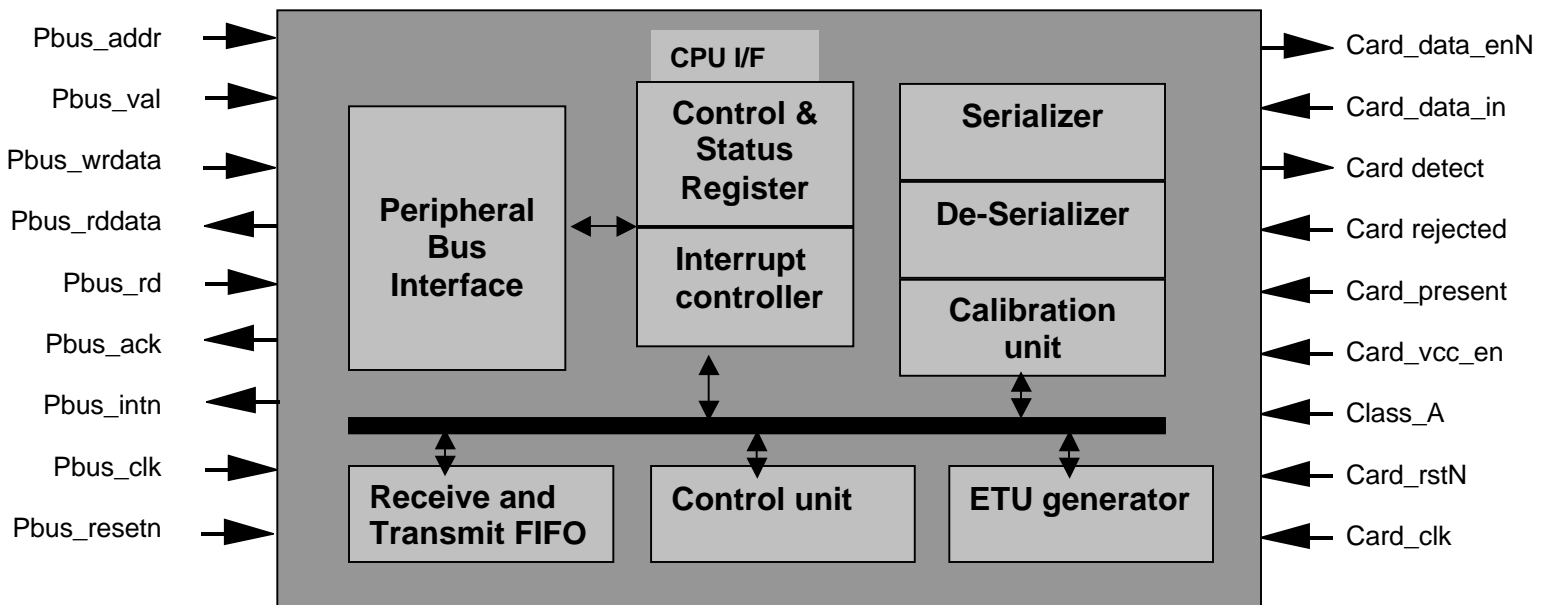
GDA's Smart card controller core is compliant to ISO 7816-3 specification. The core is a technology independent, fully synchronous design. The controller functions at 2 –66 Mhz.

The design provides a simple, timing friendly front end interface which enables easy integration of the core to controllers and other application specific front end logic.

The controller supports smart cards with internal clocks and internal resets .It has a well defined, easy to integrate processor interface. The design has hardware support for activation, deactivation and data transfer. It also supports hardware initiated smart card deactivation on card removal.

- ❑ Supports asynchronous T = 0 and T =1 transmission protocols
- ❑ Supports 2 –66 Mhz range for the input frequency
- ❑ Supports class A, B and class AB smart cards
- ❑ Timed interrupt for efficient support for synchronous protocols
- ❑ Configurable depth for data path FIFO
- ❑ Interrupts for all major events in hardware
- ❑ Data filtering for signal integrity
- ❑ C level driver for post integration SOC verification
- ❑ Technology independent
- ❑ Programmable timing parameters

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Specifications

Configurable Options

- Datapath FIFO depth
- Timing parameters

Design Attributes

- Fully synchronous
- Technology independent
- Functions at 2 to 66 Mhz
- Hardware interrupts
- Data filtering for signal integrity

Product Package

- Verilog RTL
- Verification environment
- Testcases
- Synthesis environment/scripts

Documentation

- User manual
- Verification guide
- Design document

Status: Golden [Silicon Validated]

Availability: Now

Language: Verilog

Synthesis: Synopsys DC

Simulation: Verilog XL / NC Verilog

Technology: 0.18 micron or lower

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