



# SDRAM Controller

## PRODUCT BRIEF

### Overview

### Features

GDA's SDRAM controller core is a fully synchronous, highly configurable design targeted for a wide range of applications and technologies. The design is implemented in Verilog RTL with high level of modularity.

The application dependent front end is implemented as separate module with clearly defined interface to the rest of the design. This enables quick customizing of the core for different designs.

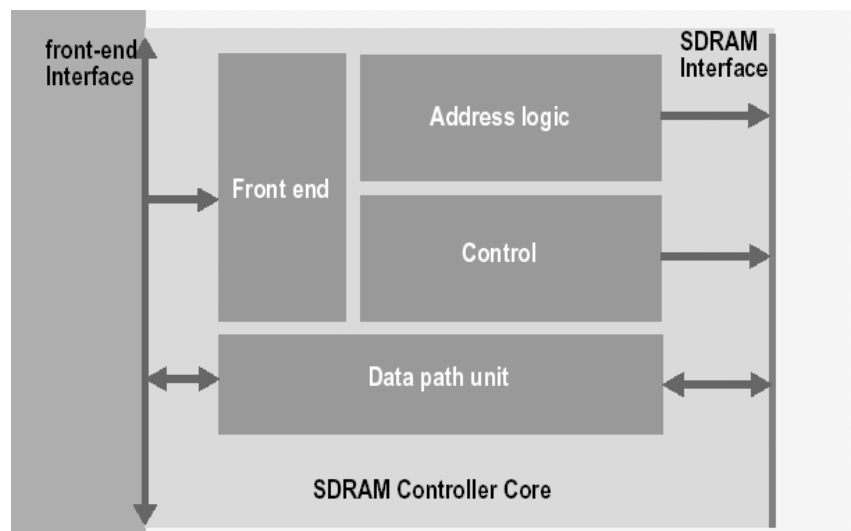
The application interface to the controller provides a completely de-coupled request and data transfer mechanisms to allow very high data bandwidth.

The interface supports a configurable number of agents, which can vary from 1 to 8. The controller architecture enables pipelining of multiple requests to improve overall memory access bandwidth.

The front-end interface is simple and timing friendly that enables easy integration of the core through on-chip buses or point-to-point connections.

- ❑ Supports >100 MHz SDRAM interface in ASIC implementations
- ❑ 6-1-1-1 burst read operation in 100 MHz
- ❑ Configurable data width and memory depth
- ❑ Supports multiple memory accessing agents
- ❑ Supports up to 8 banks of memory (CS# lines)
- ❑ Supports 16 Mbit, 64 Mbit and 256Mbit SDRAMs
- ❑ Configurable buffering on read and write paths
- ❑ De-coupled request and data lines for high data throughput
- ❑ Configurable CAS latency, burst length, number of banks and row/column address widths
- ❑ Multiple arbitration schemes for multi-agent implementations

### SDRAM Controller Core





# SDRAM Controller

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## Specifications

### Configurable Options

- Front end and SDRAM data
- Memory depth or address width
- Number of agents accessing the memory
- Depth of read and write path buffers
- Arbitration schemes: round robin, priority, time multiplexing
- Number of SDRAMs (CS# lines): 1-8
- Number of banks within SDRAM, row and column address widths
- Burst length, CAS latency
- Refresh rate, other SDRAM timing parameters

**Status: Gold [Silicon Proven]**

**Availability: Now**

**Language: Verilog**

**Synthesis: Synopsys DC**

**Simulation: Verilog XL or NC Verilog**

**Technology: 0.18 micron**

### Design Attributes

- Fully synchronous
- Technology independent
- Highly modular
- Easy to integrate, front end interface

### Product Package

- Verilog RTL
- Verification environment
- Testcases
- Synthesis environment/scripts

### Documentation

- Design
- User guide

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