



# Reed-Solomon Encoder-Decoder

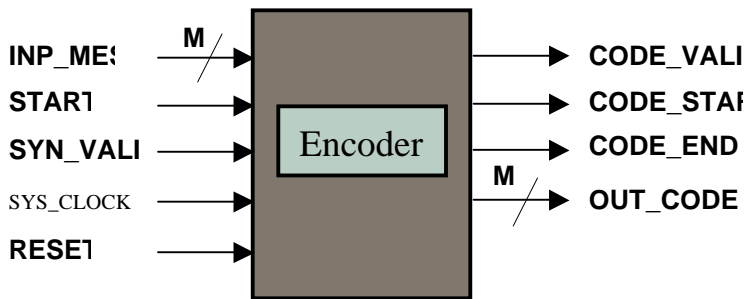
## PRODUCT BRIEF

### Overview Features

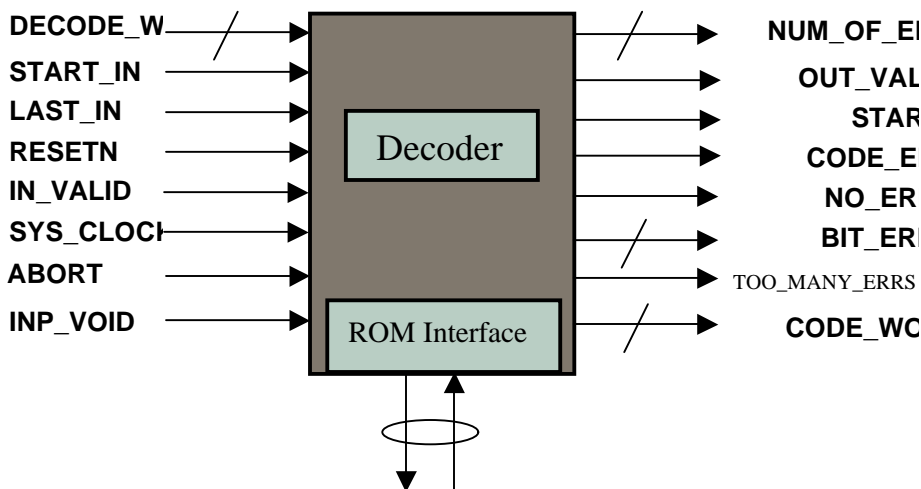
High-Performance  
Highly Configurable  
Single clock design

- High performance encoder/decoder for error detection and correction.
- Ability to detect Excess Errors.
- Fully synchronous design using a single clock supporting both synchronous/asynchronous reset.
- Per frame total bit error information available.
- ROM based design to aid high computational speed.
- Verilog pre processor code to generate configurable synthesizable verilog RTL code available.

#### Encoder



#### Decoder Overview





# Reed-Solomon

## Encoder-Decoder

**Visit:** [www.gdatech.com](http://www.gdatech.com)

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## Specifications

### Configurable Options

- Number of bits per symbol (m) (4 to 10).
- Number of data symbols per codeword (k).
- Number of parity symbols per codeword (2t).
- Primitive Polynomial.

### Design Attributes

- Highly modular design.
- Fully synchronous, technology-independent design.
- M-bit wide internal data path (M = 4 to 10).
- Single clock domain.
- FPGA Validated
- Silicon Proven

### Product Package

- RTL code and parameterized VPP code
- Detailed design document
- Verification environment
- Test cases
- Synthesis environment guide
- ROM Image files

### Documentation

- User Guide
- Verification Guide
- Synthesis Guide

**Status:** Golden  
**Availability:** Now  
**Language:** Verilog HDL  
**Synthesis:** Ambit.  
**Simulation:** Verilog-XL/NC  
**Technology:** 0.18 or better

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