



# Configurable POS-PHY Level 3 Core

## PRODUCT BRIEF

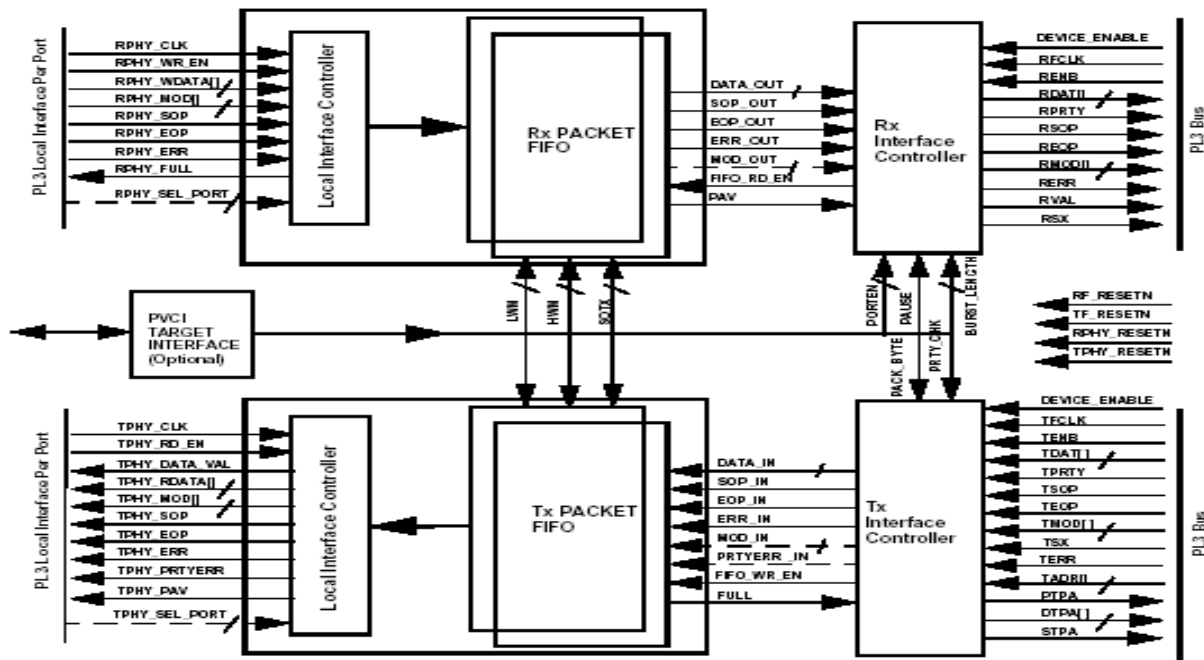
### Overview Features

#### Basic description

This Packet over SONET Level 3 (POS-PHY L3) interface allows the interconnection of Physical Layer devices to Link Layer devices in POS application. It provides a versatile bus interface for exchanging packets within a communication system. It covers all application bit rates up to and including 2.4 Gbits/s. It defines the requirement for interoperable single-PHY (one PHY Layer device connected to one Link Layer device) and multi-PHY (multiple PHY layer devices connected to one Link Layer device) applications.

#### Standard Features

- Provides a SATURN POS-PHY Level 3 compliant 8/32-bit wide data path (clocked up to 104 MHz) with internal FIFO buffers for POS-PHY channels.
- Single PHY and Multi-PHY modes, (scalable up to 255 Physical channels).
- Round-robin fashion channel selection in multi channel configuration. It also provides option to select channel from back end.
- Independent clocking for POS-PHY interface and Local interface.



Functional Block Diagram of POS-PHY Level 3 PHY Layer Core





# Configurable POS-PHY Level 3 Core

## Configurable Features

### 1) PL3 Link Layer Core

#### *Hardware features*

- Configurable bus width 8 bits or 16 bits or 32 bits at POS-PHY and local interface.
- Configurable LINK layer core for 1 to 256 channels.
- Configurable optional PVCI interface to configure the registers.
- Configurable FIFO depth.
- Configurable single or multiple local interfaces. In case of single local interface the interface is shared.
- Configurable channel addresses by position. The first channel is address 0 and last channel is address P-1. Where P is total number of PL3 channels

### Configurable POS-PHY Level 3 Core Product Brief

#### *Software features*

- Software programmable channel mask register to mask a channel. This is to control the polling of channels by appropriate masking of channels.
- Software programmable BURST LENGTH (in terms of number of bytes) for each channel. The channel selected for operation switched to the next channel after transmitting the above amount of data or after transmitting an EOP.
- Software programmable packet or byte mode of operation.
- Software programmable FIFO thresholds. Each PL3 FIFO has three thresholds that are the High water mark i.e. FIFO almost full assert, Low water mark i.e. FIFO almost full de-assert and Start of transmission i.e. FIFO almost empty threshold.
- Software programmable PAUSE between the PL3 transfers. The PAUSE can be of 0 or 2 cycles.
- Software programmable checking for no parity or odd parity over the data bus.

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