



PCI Controller Core

PRODUCT BRIEF

Overview Features

GDA's PCI controller core is a technology independent, fully synchronous, highly efficient, 32/64-bit implementation compliant to PCI Local bus specification, rev 2.2

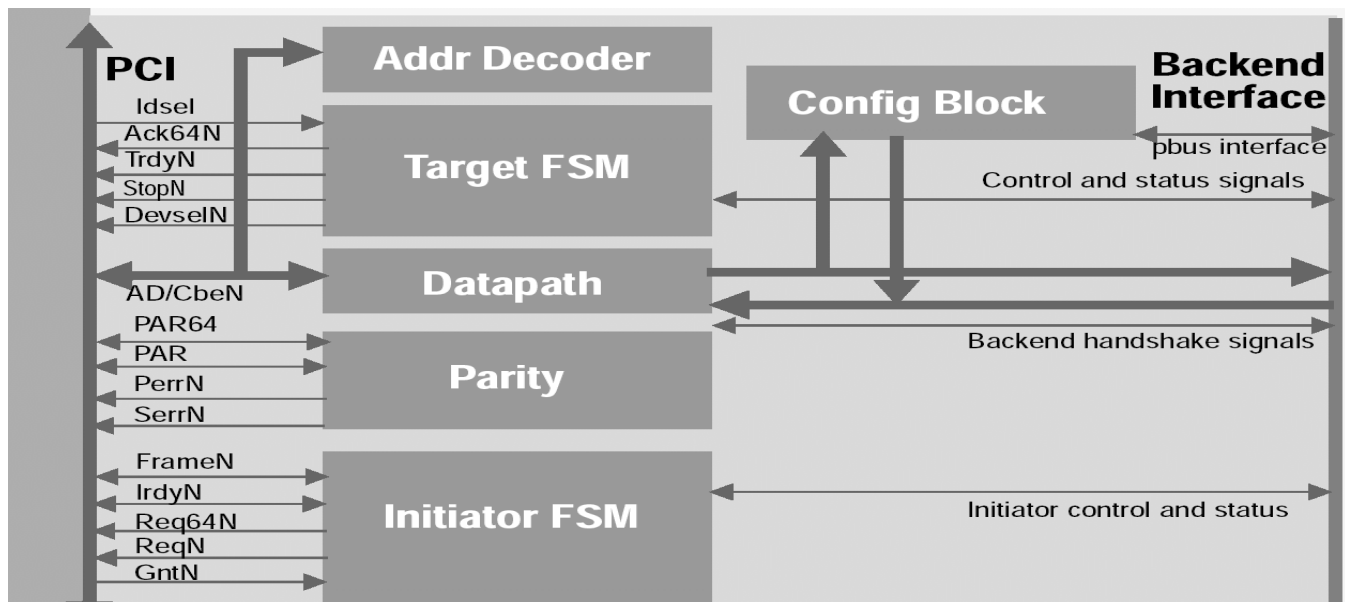
The controller is designed to function at 66 MHz in any state-of-the art ASIC technology and at 33 MHz on most FPGAs.

The design provides a simple, timing friendly backend interface that enables easy integration of the core to FIFOs, DMA controllers and other application specific backend logic.

The core provides numerous configuration options to include/exclude features to optimize the PCI interface for a particular implementation.

- ❑ Initiator (optional) and Target functionality
- ❑ Memory, IO and configuration read/write cycles
- ❑ Zero wait-state burst cycles
- ❑ Type 0 configuration header
- ❑ Medium and slow address decoding
- ❑ Target terminations: retry, target abort and disconnect with/without data
- ❑ Initiator terminations: normal termination and master abort
- ❑ Initiator latency timer
- ❑ Address and data parity error generation, detection and signaling
- ❑ Supports PCI Interrupt
- ❑ Host interface to access the configuration space from back end
- ❑ Easy to integrate back end interface
- ❑ Automatic retry for transactions terminated by target retry or disconnect
- ❑ Supports Exclusive access cycles

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Specifications

Configurable Options

- Initiator and/or target function
- 32 or 64 bit operation
- Number, type and size of BAR registers
- Address decoding medium, slow
- Memory write and invalidate command vs. memory write
- Pre-fetch vs. wait mode for target read
- Disconnect with or without data target termination
- Retry registered /combinatorial
- Parity Output registered/combinatorial
- FIFO or no FIFO in the BE
- IO transaction support
- Soft reset to back end
- Asynchronous or Synchronous reset

Design Attributes

- Fully synchronous
- Technology independent
- Highly modular
- Easy to integrate, front end interface

Product Package

- Verilog RTL
- Verification environment
- Testcases
- Synthesis environment/scripts

Documentation

- Design
- Verification
- User guide

Status: Gold [Silicon Proven]

Availability: Now

Language: Verilog

Synthesis: Synopsys DC

Simulation: Verilog XL or NC Verilog

Technology: 0.18 micron

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