



# I2S Controller Core

## PRODUCT BRIEF

### Overview Features

#### Highly Configurable Synthesizable RTL

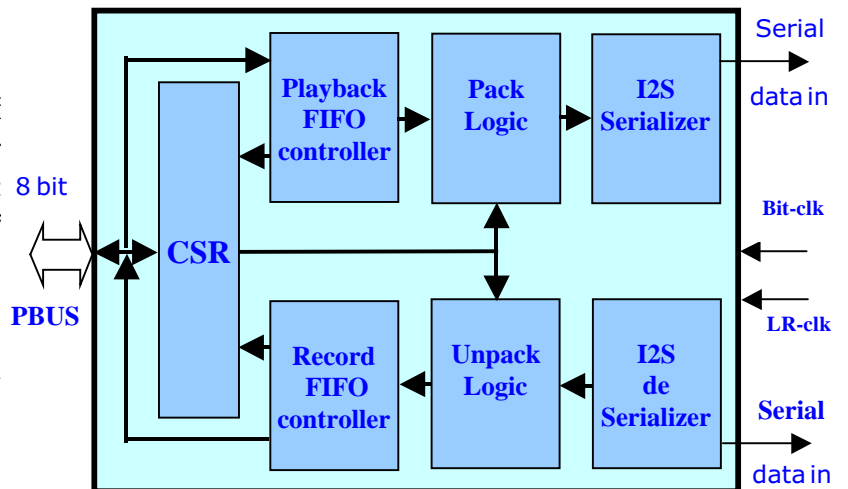
GDA's I2S Controller is a highly configurable core for use in I2S compliant CODECs. It provides a simple glueless interface to industry standard audio devices. This digital audio controller core is compliant to the dominant audio standard protocol I2S. The core is optimally architected for high performance, low latency and small silicon footprint.

The core is provided with the generic processor bus interface on the system side enabling the core to be used in a variety of applications including SoC applications. The core's simple and configurable architecture is independent of implementation tools and, most importantly target technologies. GDA's I2S core is a cost-effective, end-to-end solution that allows the licensees to easily migrate to FPGA, Gate array and Standard cell technologies optimally.

GDA's I2S core solution leverages years of experience in creating reusable designs for Ethernet, PCI-X, SPI-4 and Hyper Transport technologies to offer lowest risk in terms of compliance and interoperability.

GDA's I2S core has been tested for Amba AHB 32-bit wide interface on the system side and DMA channel support for FIFO data transfer has also been provided in this setup.

- Compliant to I2S Serial Bus protocol
- Supports full duplex flow control - 1 PCM playback channel and 1 record channel
- Supports 8/16/18/20/24/32 bit DAC/ADC resolution through software configuration
- Supports both 256 and 384 sampling frequency (fs) operating mode
- Support 8/16/32/48/96/192/44.1/88.2/176.4 KHz audio sample frequency
- Processor Bus 8/16/32-bit wide Interface on system side
- Supports 1/2/4 samples per 32 bit packing option through Software configuration
- Fully synchronous design with serial clock and system clock
- Interrupt Support for FIFO data read/write
- Programmable FIFO thresholds
- Loop back mode for testing purposes





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## Specifications

### Configurable Options

- Playback and Record FIFO depths
- Playback and Record FIFO widths
- Processor bus width – 8/16/32
- Synchronous and asynchronous reset

### Design Attributes

- Fully synchronous, technology-independent design
- Software controlled block resets and enables
- Software controlled FIFO flush
- Highly modular design: partitioned by function, timing and testability

### Product Package

- Parameterized RTL Code
- Automated and parameterized test bench
- Test cases
- Synthesis environment/scripts

### Documentation

- User Guide
- Design document
- Acceptance Test Bench Specification (ATS)
- Software specification

Status : **Verified and Synthesized RTL**  
Availability : **Available**  
Language : **Verilog HDL**  
Synthesis : **Ambit/Synplify/Xilinx**  
Simulation : **Cadence's Verilog-XL/NC Verilog**  
Technology : **0.18u or better**

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