



HDLC Controller

PRODUCT BRIEF

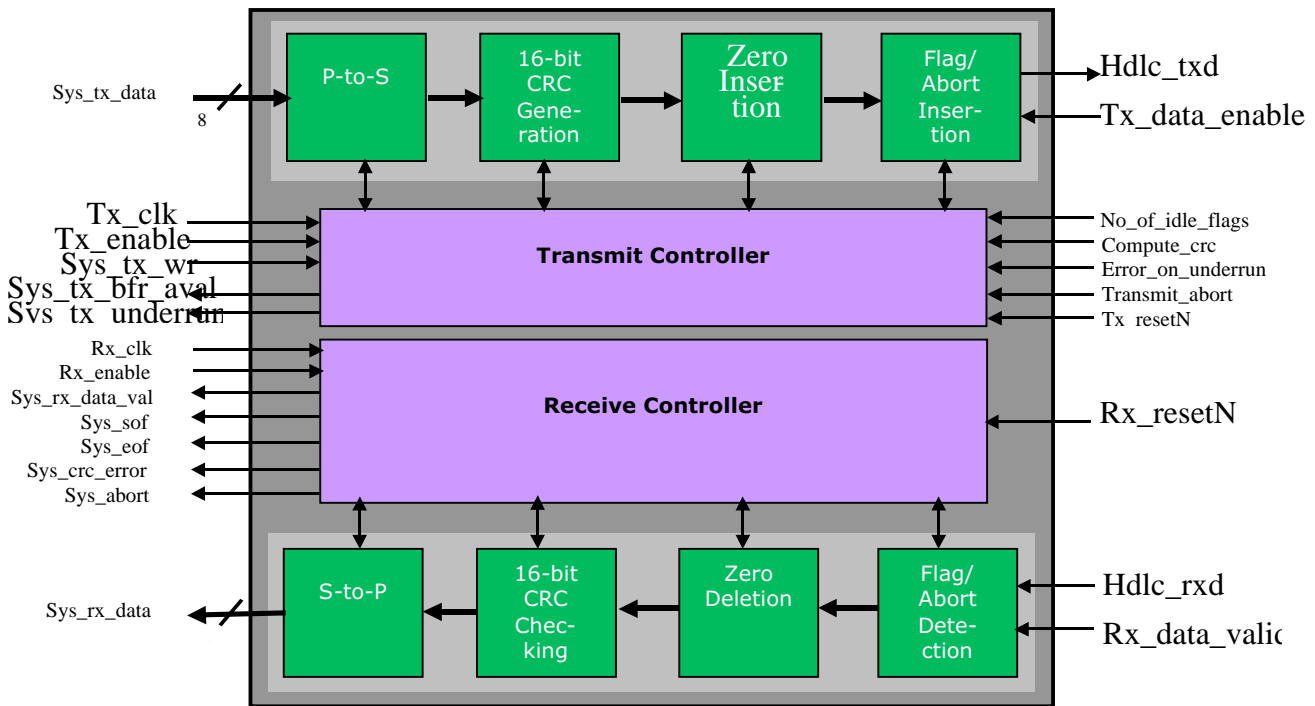
Overview Features

**Highly Configurable
Technology Independent
System Validated**

GDA's HDLC Controller is a single-channel HDLC controller core. The device contains a full-duplex transceiver with independent transmit and receive sections for bit-level HDLC protocol operations.

The core is designed for easy integration into wide range of applications implemented on most ASIC and FPGA technologies. The interface of this core can be adapted for a wide range of FIFO controllers.

- Flag insertion and detection.
- Abort generation and detection.
- Zero bit stuffing and deletion.
- 16-bit CRC-CCITT generation and checking.
- CRC can be separately enabled and disabled for transmit.
- Automatic insertion of 1 to 255 IDLE characters between frames.
- Enable and data valid signals for flow control.
- Operates up to 155.52Mbit/s (STS-3) data rates.
- Full-duplex operation.





HDLC Controller

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Specifications

Design Attributes

- Fully synchronous design
- Separate clocks for TX and Rx sections
- Highly modular design
- Advanced features such as transmit and receive
- FIFO and CRC-32 can easily be added

Product Package

- RTL code
- Automated and parameterized testbench
- Synthesis scripts

Documentation

- Design document
- Testbench Specification
- User guide

Status : Gold [Silicon proven]

Availability : Now

Language : Verilog

Synthesis : Synopsys DC

Simulation : Verilog XL / NC Verilog

Technology : 0.18-micron

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August 2003 Version 1.0

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