



PCI-Express / Advanced Switching Interface Controller



PRODUCT BRIEF

Overview Features

Highly Configurable, Multi Protocol Chip-to-chip and Board-to-board High Performance

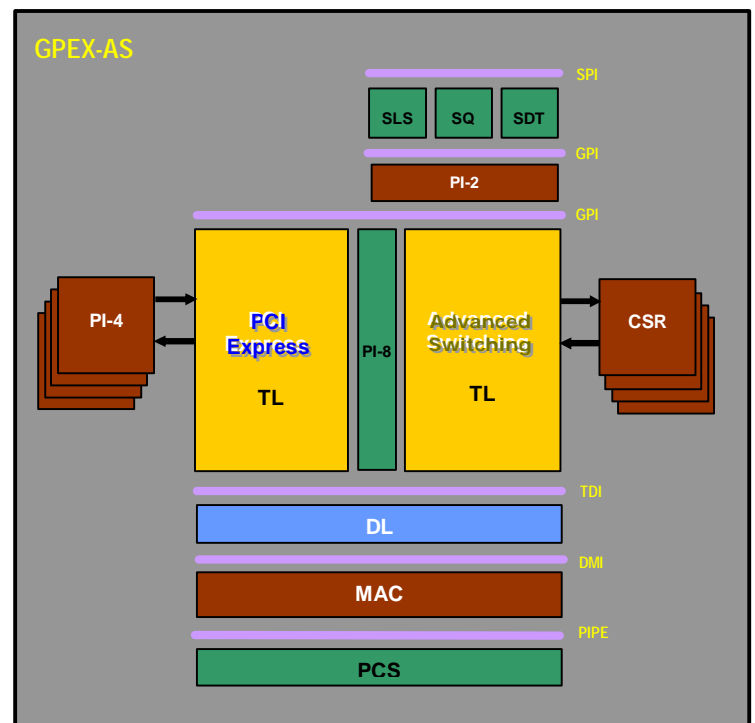
GPEX-AS is a highly flexible and configurable end point controller IP targeted for both PCI-Express and Advanced Switching technology implementations in compute and communication applications. GPEX-AS is part of GDA's PCI-Express (GPEX) family of IP solutions which includes End Point (GPEX-EP) and Root Complex (GPEX-RC) designs.

GPEX-AS supports both PCI-Express and AS protocols. It supports PCI-express end-point and root complex functions, and AS port controller logic for a wide range of applications such as native AS node, leaf bridge, root bridge and switch. The controller architecture is tailored to address the needs of different market segments with highly configurable system PIs and support for PI-8, SLS, SQ and SDT.

GPEX-AS architecture offers High performance, High link utilization, Low latency, Low power consumption and Small silicon footprint. It's simple, configurable, layered architecture is independent of application logic, PHY designs, implementation tools and the target technology. It can be easily used in FPGA, Gate Array and Standard Cell technologies optimally.

The GPEX-AS IP core leverages the years of experience in PCI, PCI-X, Hyper Transport and PCI-Express technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and interoperability. GDA is a leading IP provider for high-speed interconnect technologies, with several licenses sold in compute, storage and networking markets.

- Compliant with AS Core Specification V1.0
- Compliant with PCI-Express Base Specification V1.0a
- Compliant with PI-8, SLS, SQ and SDT specification V1.0
- Compliant with PIPE Architecture Specification V1.0
- Targets end-point, switch and bridge implementations
- Optimally supports data rates ranging from 2G to 40G
- Optimized for high link utilization and low latency
- Supports up to 8 BVCs, 8 OVCs and 4 MVCs
- Hardware assistance for system PI functions
- Hardware assisted congestion management support
- Efficient buffer management and flow control
- Targets both FPGA and ASIC technologies





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Specifications

Configurable Options

- ✍ PCI-Express, AS or Both
- ✍ Maximum link width (x1, x2, x4, x8, x16)
- ✍ Inclusion of System PIs PI-8 SLS SDT SQ
- ✍ Number of virtual channels
- ✍ Buffer size for each virtual channel
- ✍ Data path width 32 / 64 / 128
- ✍ VC arbitration scheme
- ✍ Maximum payload size
- ✍ Number of Connection Queues

Design Attributes

- ✍ DFT friendly, Fully synchronous design
- ✍ Layered Architecture
- ✍ Sync or Async Reset support
- ✍ Clearly demarked clock domains
- ✍ Software control for key features

Product Package

- ✍ RTL view in Verilog HDL
- ✍ Comprehensive functional test bench
- ✍ Synthesis scripts
- ✍ Compliance checklist test suite
- ✍ Training and support programs

Documentation

- ✍ Data Sheet
- ✍ Design Guide
- ✍ Verification Guide
- ✍ Synthesis Guide

Availability : Q204 – DL, MAC, TL
Q304 – SLS, SQ, PI-8
Q404 – SDT

Language : Verilog HDL

Synthesis : Synopsys DC

Simulation : Verilog-XL/NC Verilog

Technology : ASIC 0.18u or better, FPGA

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