



HyperTransport Tunnel



PRODUCT BRIEF

Overview Features

High-Speed
Low-Latency
Point-to-Point Link

HyperTransport technology is a high-speed, low-latency, point-to-point link for interconnecting integrated circuits (ICs) on a board. It is a packet-based link implemented on two independent unidirectional sets of wires.

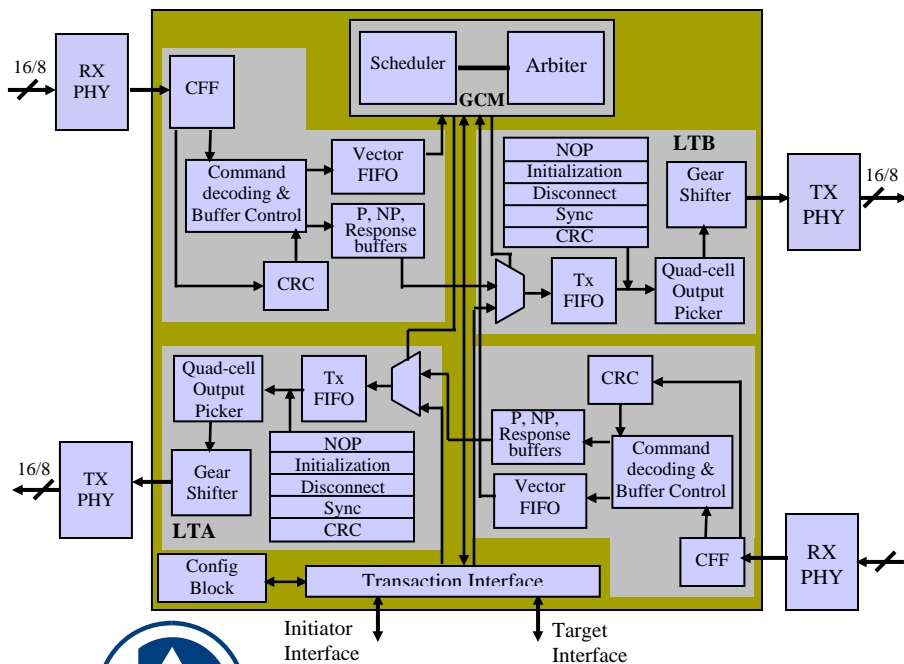
GDA's HyperTransport Tunnel core is designed for reuse and its flexible backend interface makes it easy to be integrated into wide range of applications. The core provides highly scalable upstream and downstream bandwidths through programmable link widths and frequencies.

HyperTransport Tunnel core meets today's demand for the increased bandwidth and offers more bandwidth than any existing solutions. The upstream link could be run 24 times faster than a 32 bit, 33 MHz PCI bus. The core is designed to operate the upstream link at up to 1200 MHz DDR, yielding an effective transfer rate of 2.4 Gbits per second per wire pair. The design targets networking, telecommunications, embedded systems and any application where high speed, low latency response, low pin counts and scalability are necessary.

GDA's HyperTransport Tunnel solution leverages years of experience in PCI, PCI-X, and PCI Express technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and interoperability. GDA is a leading IP provider for high-speed interconnect technologies, with several licenses sold in compute, storage and networking markets.

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- Proven design compliant with HyperTransport I/ O Link specification, Rev. 1.1
- Provides dual HyperTransport links and either link can be hardware configured for 16- bit or 8-bit link interface
- Either link supports software programmable link widths of 16, 8, 4, or 2bits.
- Either link can be configured as upstream
- Either link supports 1200, 1000, 800, 600, 500, 400, or 200 MHz link frequencies
- Maximum bandwidth is 9.6 GB/sec on both links
- Supports independent link width and frequency for each link
- Supports direct peer-to-peer traffic
- Supports greater concurrency using unitID clumping
- Supports 16 streaming virtual channels
- Supports error handling through retry mechanism
- Supports 64 bit addressing
- Backward compatible with all previous revisions of HT
- Supports link disconnect protocol and interrupt
- Supports external and internal loop backs on both HT links
- Transaction interface provides target and initiator interfaces



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HyperTransport Tunnel

Availability : April 2004
Language : Verilog HDL
Synthesis : Design Compiler
Simulation : Verilog-XL/NC, VCS
Technology : 0.13u Standard Cell

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January 2004 Version 1.0

Specifications

Configurable Options

- Link Widths: 16/8 bits
- Data path widths: 64/128
- Back-end interface can be configured to transaction interface
- Transaction interface can be configured to support target interface only
- Configurable buffer size for each virtual channel

Design Attributes

- Highly modular design
- Fully synchronous, technology-independent design
- 128-bit wide internal data path
- Most part of the Tunnel logic operates at 200 MHz core clock or more
- Clearly demarked clock domains
- Active-low asynchronous reset

Product Package

- RTL code
- Detailed design document
- Verification environment
- Test cases
- Synthesis environment/scripts

Documentation

- Design Guide
- Verification guide
- Synthesis guide

