



Gigabit Ethernet MAC

PRODUCT BRIEF

Overview Features

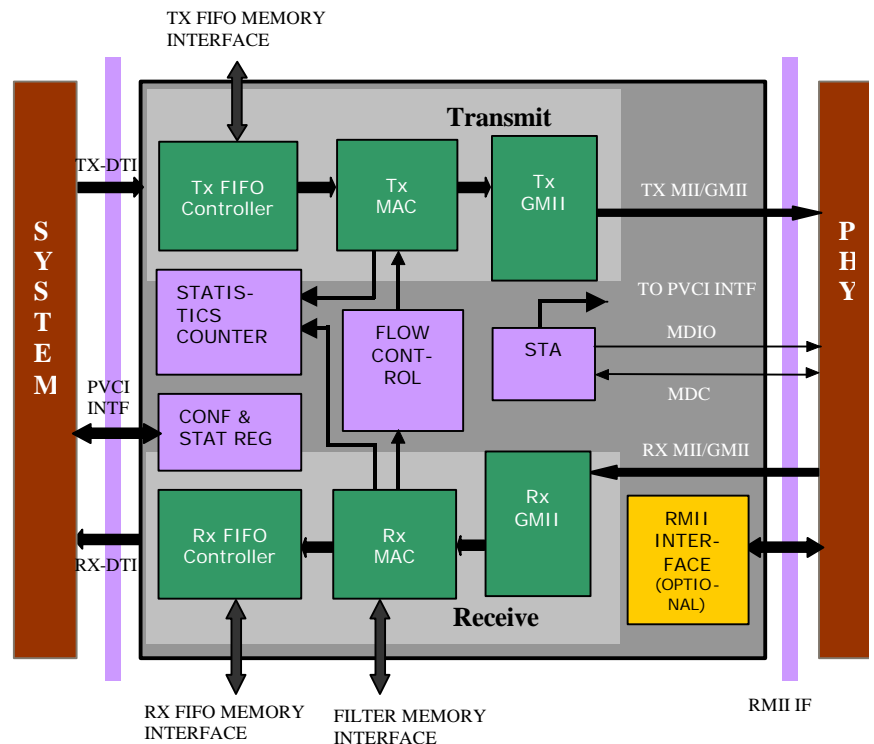
**Highly Configurable
Technology Independent
System Validated**

The Gigabit Ethernet Media Access Controller (GEMAC) ASIC core is a macro designed to use in switching, routing, up-links, server adapters and other SOC applications. The controller architecture is carefully tailored for high throughput, low latency, better reliability, low power consumption, and small silicon footprint.

The controller's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. GDA solution allows the licensees to easily migrate to FPGA, Gate array and Standard cell technologies optimally. Its flexible backend interface makes it easy to be integrated into wide range of applications. The GDA solution provides highly scalable bandwidth through configurable lanes, widths and frequencies. The GEMAC core is highly configurable, fully synchronous, and highly modular design to meet the requirement of a reusable IP in SoC designs.

GDA's GEMAC solution leverages years of experience in 10/100 Mbps MAC, SPI-4, PCI-X, and Hyper Transport technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and inter operability.

- Gigabit Ethernet Media Access Controller compliant to IEEE 802.3 specifications
- Supports 10/100/1000 Mbps PHY devices with auto-negotiation feature
- Supports full duplex flow control
- Supports half duplex for 10/100 Mbps operation
- Supports VLAN - compliant to IEEE 802.1Q
- MII/GMII interface on line side
- 32-bit wide, point-to-point interface (DTI) on system side
- Configurable depth for Tx and Rx FIFOs
- Store-and-forward and cut-through modes of operation
- Jumbo and short frame support
- Statistics counters for RMON, SNMP, and 802.3





Gigabit Ethernet MAC

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Specifications

Configurable Options

- Optional Half Duplex feature
- Optional support for 10/100 Mbps along with 1000Mbps
- Receive and Transmit FIFO depths
- Size of the Multicast and VLAN hash tables
- Number of exact MAC addresses for receive packet filtering
- Inclusion of number of pattern match filters
- Inclusion of statistics counter and PHY management logic (STA)

Design Attributes

- Fully synchronous design, 8-bit data path
- Software controlled block resets and enables
- Highly modular design: partitioned by function, timing, and testability.
- Separate hierarchy for optional logic to aid ease of removal
- Most of the logic operates up to 125Mhz clock frequency

Product Package

- Parameterized RTL Code
- Automated and parameterized test bench
- Parameterized synthesis scripts.
- Reports and scripts of Code coverage

Documentation

- Functional Requirement Specifications.
- Test bench Specifications
- Acceptance Test Specifications
- User guide for core integration, simulation, and synthesis

Status : Verification & Validation Phase
Availability : July 2003
Language : Verilog HDL
Synthesis : Ambit/Synopsys
Simulation : Cadence's Verilog-XL/NC Verilog
Technology : 0.18u or better

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August 2003 Version 1.0

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