

# Xilinx V-5, PCI Express Gen1/Gen2 and USB3.0 IP-VP

## HIGHLIGHTS

- Xilinx Virtex-5 High-speed FPGAs
- Two Gigabit Ethernet ports
- Two x4 PCI Express
- Support for PCI express Gen1/Gen2
- Support for USB 2.0/USB 3.0.
- 8Gb ONFI 2.0 NAND Flash

## APPLICATIONS

Ideal platform for prtotyping in the following:

- Data storage
- Mobile computing
- High Speed Data Centers

### IP Validation for

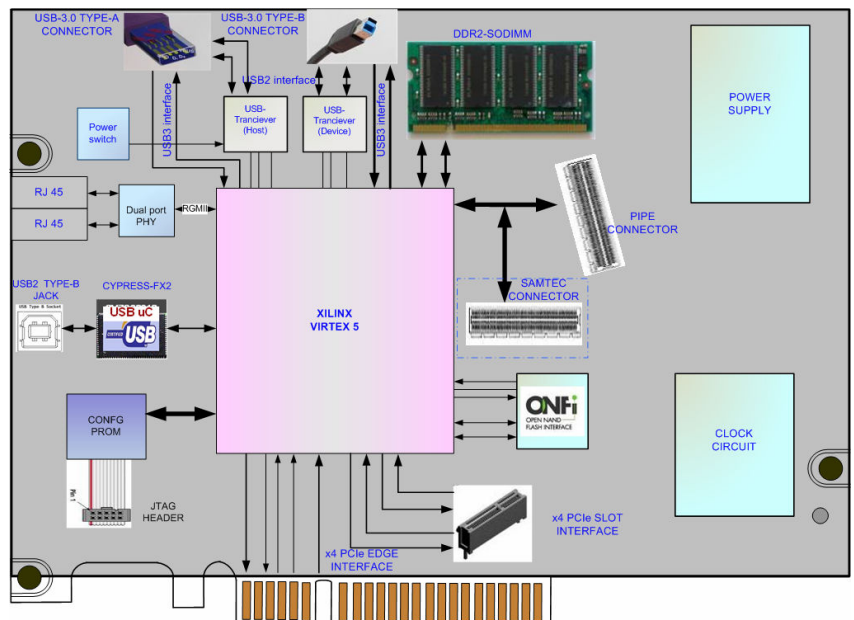
- USB 3.0/ USB 2.0,PCI Express Gen1/Gen2 & PIPE.
- DDR2 memory controller

IP-VP (IP- Validation Plat form) is available with options of latest Xilinx Virtex-5 LXT/FXT series of FPGAs.GDA07KB802B-IP-VP is an ideal platform for Prototyping and IP validation for High-speed I/O interfaces.

Virtex-5 FPGA RocketIO GTX/GTP Transceivers Have been used to support High speed interface lanes for PCI Express Gen1/Gen2 ,PIPE and USB3.0/USb 2.0.

2 USB ports Supports USB3.0/USB2.0, Host, Device.

One on board Loop back provision also provided For IP Validation.



8Gb ONFI NAND Flash interface is provided to enable Bulk data transfer.

The 200-pin (Non ECC) SO-DIMM provides access to up to 2 GB of DDR-II memory Interface.

Two Gigabit Ethernet interface ports with Broadcom RGMII PHY to enable High speed network interface.



## **TECHNOLOGY FEATURES**

### **Supported FPGAs**

→ Xilinx XC5VLX110T, XC5VLX220T & XC5VLX330T (1738)  
High-performance logic with advanced serial connectivity.

→ Xilinx XC5VFX100T  
High-performance embedded systems with advanced serial connectivity

### **PCI Express Interface**

- Two x4 PCI Express Interfaces.
  - x4 PCI Express Edge Connector.
  - x4 PCI Express Slot Connector.
- Compliant with the PCI Express Gen1 with V-5 LXT Devices.
- Compliant with the PCI Express Gen2 with V-5 FXT Devices.

### **Universal Connectivity**

→ Two USB 3.0 Ports  
One USB2.0/USB3.0 Host interface Port with standard USB 3 Type A connector.

One USB2.0/USB3.0 Device interface Port. with standard USB 3 Type B connector.

→ One USB LOOP BACK Port.

→ One USB2.0 compliant Host interface (for management access to FPGA logic) through Cypress USB Micro controller

→ 2 Gigabit Ethernet interface.

→ JTAG Test access Port.

### **Memory Interface.**

→ 200 Pin (64-bit) SODIMM interface for DDR-II.

→8Gb ONFI 2.0 NAND Flash interface.

### **Clocking.**

→ MGTX Dual tile Reference Clock is generated with PCI Gen1/Gen2 compliant selectable frequency Jitter attenuator/Synthesizer.

### **Packaging /Power.**

### **Ordering.**



**GDA Technologies, Inc.**  
accelerate your innovation™  
( An L&T Infotech Company )

1010, Rincon Circle, San Jose, CA 95131  
Tel 408 432 3090. Fax 408 432 3091  
Email : sales@gdatech.com. www.gdatech.com

