



## Overview

GDA's configurable multi-channel DMA controller (CDMAC) can have upto 32 channels. Each channel can be hardly configured to function in descriptor or conventional mode of operation. The 4 channel conventional mode configuration makes the CDMAC to function as intel 8237 device. Additionally, descriptor mode channels can be configured by the software to function in the conventional mode.

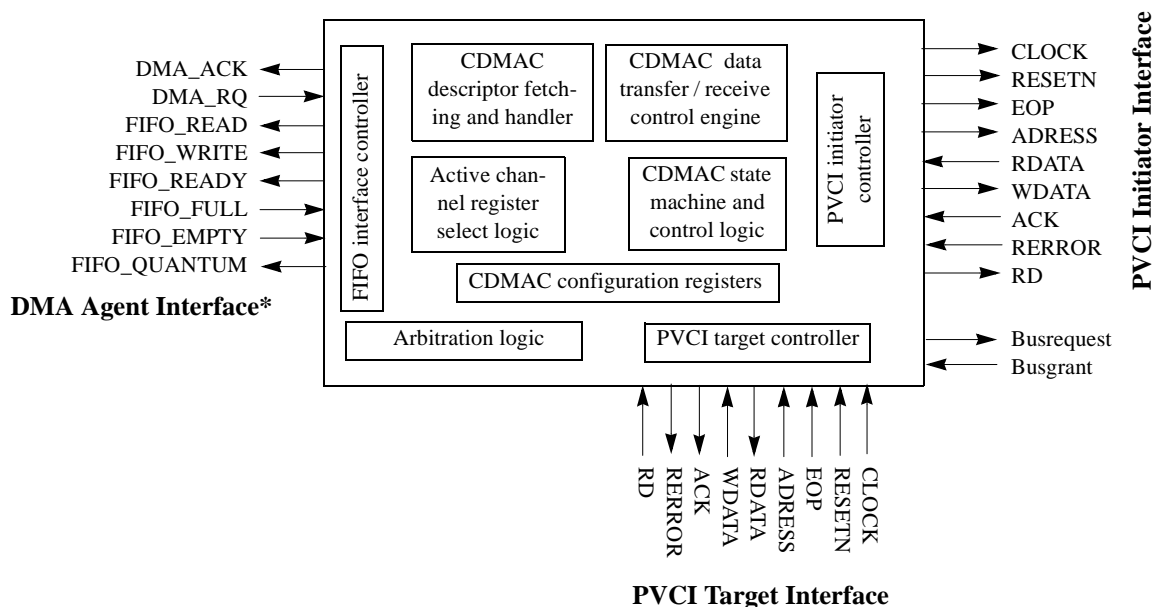
The CDMAC used the simple and generic PPCI interfaces. The PPCI target is used for the software configuration and initialization. The PPCI initiator is used for the DMA transfers.

The CDMAC can be used in varied applications using its different software and hardware configurable features. The CDMAC channels configured for conventional mode of operation is used to service slow peripherals and low-bandwidth requirement devices like UART, IEEE-1284, IIC-interface devices, FDC (floppy discontroller) and audio applications. In such applications, CDMAC is a low priority, secondary bus device. The CDMAC communicate with its local secondary bus memory directly or to the system memory through the secondary to primary bus bridge. The CDMAC channels configured in descriptor mode can be used to service the high speed and high bandwidth devices like USB, IEEE-1394 device, high speed DSP or video applications. In such applications, CDMAC is a primary bus device and communicates directly with primary memory and is allotted the higher priority by the bus controller.

### Standard features

- Supports all standard modes of DMA operation like burst-mode, block-mode and single data-unit transmission.
- Peripheral Virtual Component Interface (PPCI) based hardware interface can be easily plugged into any system.

- The DMAC supports non-interfering and non-blocking multi-channel functionality up-to a maximum of 32 channels.
- Provides the flexibility to the vendor to plug in its own FIFOs externally in the design at the agent interface.
- In 4 channel conventional mode of operation, CDMAC maintains total software and hardware compatibility with intel 8237 device.



**FIGURE 1. CDMAC Block diagram description**

\* Agent interface is per channel interface



## **Configurable Features**

### ***1. Hardware features***

- Provides flexibility for 8-bit, 16-bit and 32-bit transmission/receive of data.
- Flexibility to configure address bus size and internal counter/register sizes is also provided for effective resource usage by the DMAC.
- Each of the channel is configured to support either the Open Host Controller Interface i.e. descriptor based operation or conventional.
- The DMA controller can handle both the fast and slow peripheral devices by the use of synchronization circuitry and handshake mechanism.

### **Product Package**

- Parametersied RTL Code
- Automated and parameterised testbench.
- Parameterised synthesis scripts.
- Reports and scripts of Code coverage.

### ***2. Software features***

- Reduced interrupt load on the system in both Conventional DMA mode and Open Host Controller Interface Mode provided by highly configurable interrupt routing mechanism that is configurable by the software.
- Software configurable round robin and priority arbitration scheme for channel selection.
- Software can easily diagnose the errors occurred during the transaction on a particular channel by accessing the DMAC register set.
- The DMAC supports the 8-bit, 16-bit, 32-bit software configurable data width at the agent interface.

### **Documentation**

- Functional Requirement Specifications.
- Architecture Specification.
- Test bench specification
- Acceptance Test Specification
- User manual for installation and programming.

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**Status** : Complete  
**Language** : Verilog HDL  
**Size** : Approx. 5k gates (4 channels)

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